WHAT IS CLAIMED IS:

1. A method for verifying the hardware operation of an Application Specific Integrated Circuit ("ASIC") chip having microcode logic for enabling Transmission Control Protocol/Internet Protocol ("TCP/IP") processing, said method performed in a system that comprises a first computing device having a processor and register transfer level (RTL) code for simulating a computing device that includes said ASIC, said system further comprising a second computing device coupled to said first computing device via a network, said second computing device comprising a processor and a TCP/IP stack for performing TCP/IP processing, said method comprising the steps of:

(a) causing said RTL code to initiate a TCP/IP connection between said first computing device and said second computing device over said network, including the generation of a SYN packet addressed to said second computing device that is coupled by said first computing device to said network so as to enable said SYN packet to be received and processed by said second computing device;

(b) detecting by said first computing device a SYN-ACK packet generated by said second computing device in response to its receipt of said SYN packet; and

(c) causing said RTL code to process said SYN-ACK packet and to generate an ACK packet that is coupled by said first computing device to said network for receipt by said second computing device, so as to complete said RTL code initiated TCP/IP connection.

2. The method of Claim 1 further comprising the steps of:

(d) causing said first computing device to detect on said network a SYN packet addressed to said RTL code, thereby recognizing that said second computing device has initiated a TCP/IP connection between said first computing device and said second computing device over said network, and for coupling said SYN packet to said RTL code;

(e) processing said SYN packet by said RTL code, and causing said RTL code to generate a SYN-ACK packet that is coupled by said first computing device to the network so as to enable said SYN-ACK packet to be received by said second computing device; and

(f) detecting by said first computing device an ACK packet generated by said second computing device in response to its receipt of said SYN-ACK packet, so as to complete said second computing device initiated TCP/IP connection.

3. The method of Claim 1 wherein said RTL initiated TCP/IP connection enables the transfer of at least one packet of data between said first computing device and said second computing device.

4. A system for verifying the hardware operation of an Application Specific Integrated Circuit ("ASIC") chip having microcode logic for enabling Transmission Control Protocol/Internet Protocol ("TCP/IP") processing, said system comprising:

a first computing device having a processor and register transfer level (RTL) code for simulating a computing device that includes said ASIC; and

a second computing device coupled to said first computing device via a network, said second computing device comprising a processor and a TCP/IP stack for performing TCP/IP processing, wherein: said RTL code is designed to initiate a TCP/IP connection between said first computing device and said second computing device over said network, including the generation of a SYN packet addressed to said second computing device that is coupled by said first computing device to said network so as to enable said SYN packet to be received and processed by said second computing device; said first computing device is operative to detect a SYN-ACK packet generated by said second computing device in response to its receipt of said SYN packet; and said RTL code is designed to process said SYN-ACK packet and to generate an ACK packet that is coupled by said first computing device to said network for receipt

by said second computing device, so as to complete said RTL code initiated TCP/IP connection..

5. The system of claim 4, wherein: said first computing device is further operative to detect on said network a SYN packet addressed to said RTL code, thereby recognizing that said second computing device has initiated a TCP/IP connection between said first computing device and said second computing device over said network, and for coupling said SYN packet to said RTL code; said RTL code is further designed to process said SYN packet to generate a SYN-ACK packet that is coupled by said first computing device to the network so as to enable said SYN-ACK packet to be received by said second computing device; and said first computing device is further operative to detect an ACK packet generated by said second computing device in response to its receipt of said SYN-ACK packet, so as to complete said second computing device initiated TCP/IP connection.

6. The system of Claim 4 wherein said first computing device and said second computing device are connected via one or more Local Area Networks.

7. The system of Claim 4 wherein said RTL code is Verilog code and at least one TCP/IP timer value in said second computing device is slowed to enable said Verilog code to respond to a packet sent by said second computing device before said second computing device times out and retransmits said packet.

8. The system of Claim 4 wherein said first computing device is a Sun workstation and said second computing device is a Linux machine, and said system further comprised a third computing device that is a Linux machine, said third computing device coupled between said first and second computing devices, wherein said third computing device is operative to receive at least one packet from said first computing device addressed from said RTL code to said second

computing device and to place each said packet on the network, said third computing device is further operative to look for at least one packet from said second computing device addressed to said RTL code and to forward each said packet to said first computing device.